HOWARD COLLEGE, UNIVERSITY OF KWAZULU-NATAL, DURBAN

Analogue Electronics – 1 (ENEL3TA-H1)

Year - 3 / Semester- 1 / 2026, Main Examination

Sr. No.	DO NOT WRITE IN THIS AREA	Student number:

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Internal Examiner: Dr Bhekisizwe Mthethwa

Date: 05 June 2026 (Friday) **Time: 2 hours**
TOTAL MARKS: 70 marks
Instructions:
1. This is a closed-book examination. You can use a Calculator.
2. You are not allowed to use any notes or textbooks to assist you to answer the questions.
3. Write your answers in the space provided on the question paper.
4. Show all calculations on the question paper clear pages.
5. **Untidy work will not be marked**.
6. Please answer **ALL** the questions in the question paper

QUESTION 1 (Current Mirrors) [10 marks]

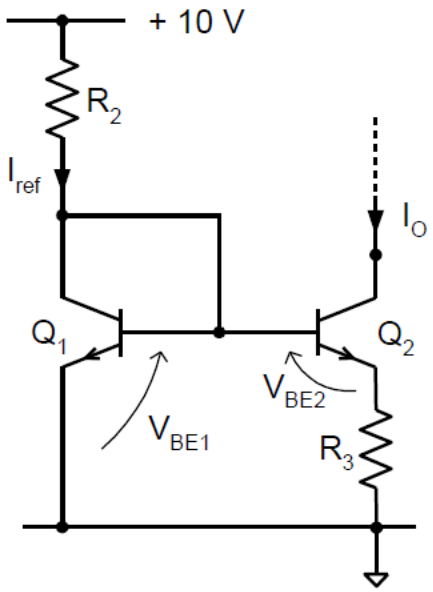

Fig. 1, "A Widlar current mirror"

a) Derive the incremental resistance as seen looking into the base of the diode connected BJT Q_1 in Fig. 1. **[4 marks]**

b) Hence, derive the output resistance as seen from the output collector terminal of BJT Q_2 of the Widlar current mirror in Fig. 1. **[6 marks]**

QUESTION 2 (Differential Pair Amplifiers) [15 marks]

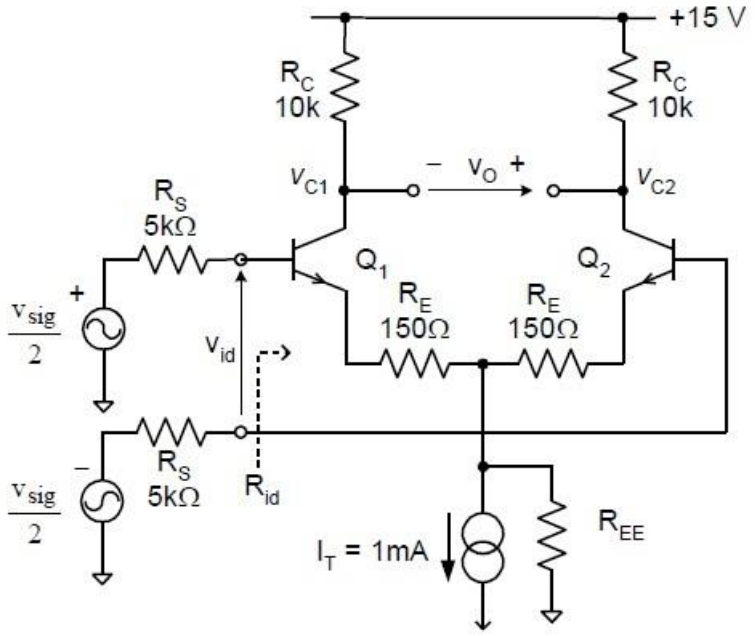

Fig. 2, "Differential Pair Amplifier with Wilson Current Mirror"

The differential amplifier shown in Fig. 2 uses matched transistors with $V_{BE} = 0{,}7\ V$ and $V_T = 25\ mV$. The DC forward current gain for **ALL** BJTS is $\beta = 100$. The differential amplifier in Fig. 2 is DC biased by a Wilson current mirror with a biasing tail current of $I_T = 1mA$. The matched BJTs used to construct the Wilson current mirror have a $\beta = 100$ and an Early voltage parameter of $4V$.

i) Assuming the amplified pure differential **open-circuit** output differential voltage is as shown in Fig. 2 as V_o. Assuming that we connect the load resistance of $20k\Omega$ to the differential output terminals of the differential pair in Fig. 2, what is the output differential voltage expression, **under load conditions**, with respect to the **open-circuit** output differential voltage V_o.

[**2 marks**]

ii) Based on your answer in 2 i), how would you **modify** the circuit in Fig. 2 with the objective to **maximize** the open-circuit output differential voltage transfer to the load resistance of $20k\Omega$ with minimal losses. [**2 marks**]

iii) When conducting an electromagnetic interference experiment on the differential amplifier in Fig. 2, it is noticed that the differential output voltage has a very noisy output. The input signal is correctly supplied using differential pair cabling and the signaling is indeed differential signaling. Explain how you would **modify** Fig. 2 with the objective to **minimize** the effect of the electromagnetic interference picked up by the input differential signal cabling connected to the input of the circuit in Fig. 2? [**3 marks**]

iv) After modifying the circuit in Fig. 2 based on your answer in 2 ii), we replace the $20k\Omega$ load resistor with a low power ear-pod with input resistance of $20k\Omega$. We then realize that the audio differential input signal V_{sig} into the differential amplifier in Fig. 2 is not transferred efficiently due to input losses. Explain, **including relevant calculations**, what is causing the input losses and hence inefficient transfer of the audio differential input signal V_{sig} into the amplifier as V_{id} in Fig. 2? [**7 marks**]

v) Recommend how you would modify the circuit in Fig.2 to alleviate the issue raised in question 2 iv) [**1 mark**]

QUESTION 3 (Filters and Filter Design) [20 marks]

a) You are a Navy soldier inside a nuclear submarine and you want to detect objects under seawater using SONAR technology. The SONAR technology works by emitting soundwaves in the ultrasound frequency range of 25kHz to 95kHz. Since the reflected SONAR signals, received from under water objects, are weak in nature; the received reflected signals must be amplified **uniformly** within the 25kHz to 95kHz passband frequency range. The **uniform/constant** gain to be applied between the 25kHz and 95kHz passband is 20dB. It is desired that the **linear** passband gain losses 29.3% of its gain at the SONAR signal frequencies of 20kHz and 100kHz. **Derive a transfer function** for the **appropriate** filter that will meet these specifications assuming the maximum passband ripple is 3dB and the filter order is 2. **Draw the necessary diagrams to design the filter if need be. Also name the type of filter being designed.** [**8 marks**]

b) Using only passive R-C filter circuits and any other necessary active circuitry, implement the transfer function derived in 3a) and draw the final circuit with correct component values. Assume a suitable value for the resistors in the R-C circuits based on the advice given in Class. [**5 marks**]

c)

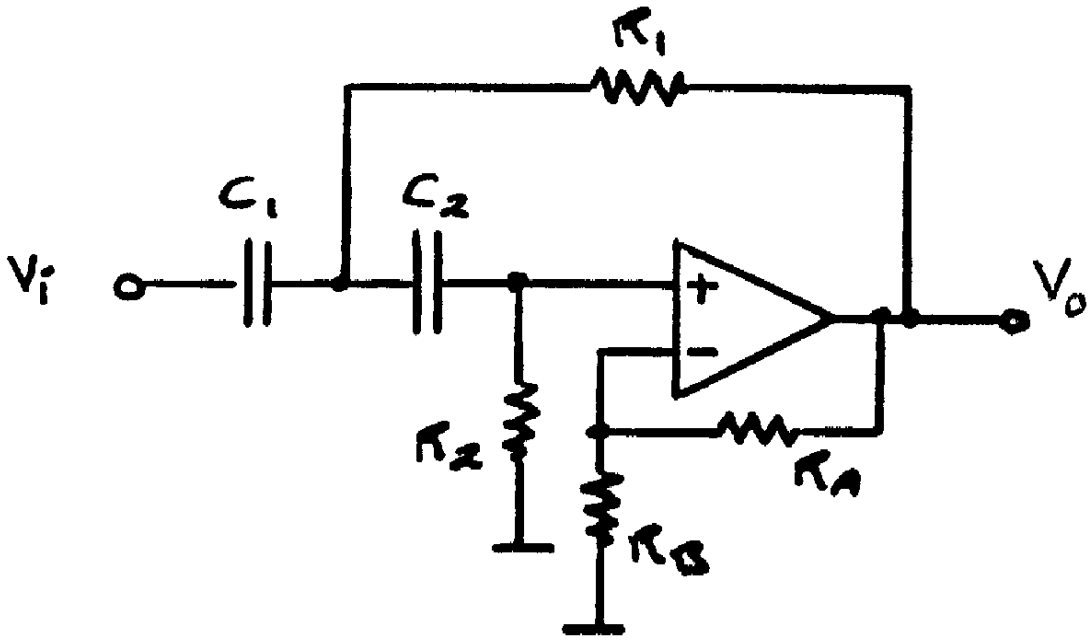

Fig. 3, "2nd order Filter"

Using the tools of analysis of inductive and capacitive reactance, amongst other tools, answer the following questions:

i) What type of filter (**high pass, low pass or band-pass**) is the circuit in Fig. 3 and why? [**3 marks**]

ii) Derive the **passband** voltage gain of the filter, in Fig. 3, assuming the OP-AMP is **ideal**. [**4 marks**]

QUESTION 4 (CMOS and MOS Technology) [15 marks]

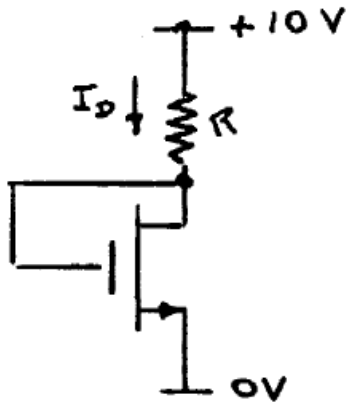

Fig. 4, "MOSFET circuit with negative feedback DC biasing"

Given that the threshold voltage of the N-MOS MOSFET in Fig. 4 is $V_{tn} = 2V, \lambda = 0,$ and $k_n' \left(\frac{W}{L}\right) = 200\mu A/V^2$ then:

a) Design the circuit so that $I_D = 0.4mA$. Determine resistance R and V_D. [**6 marks**]

b)

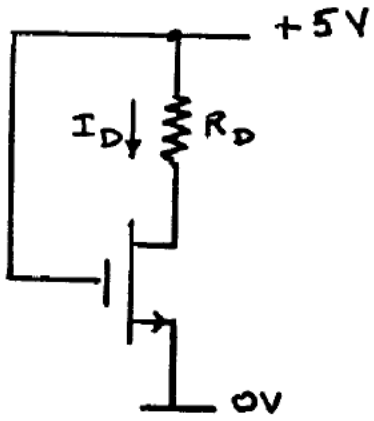

Fig. 5, "MOSFET circuit with DC biasing."

The threshold voltage of the N-MOS MOSFET in Fig. 5 is $V_{tn} = 1V$ and $k_n' \left(\frac{W}{L}\right) = 1mA/V^2$.

Design the circuit so that the DC quiescent drain voltage is $0.1V$, hence, determine R_{DS}. [**5 marks**]

c)

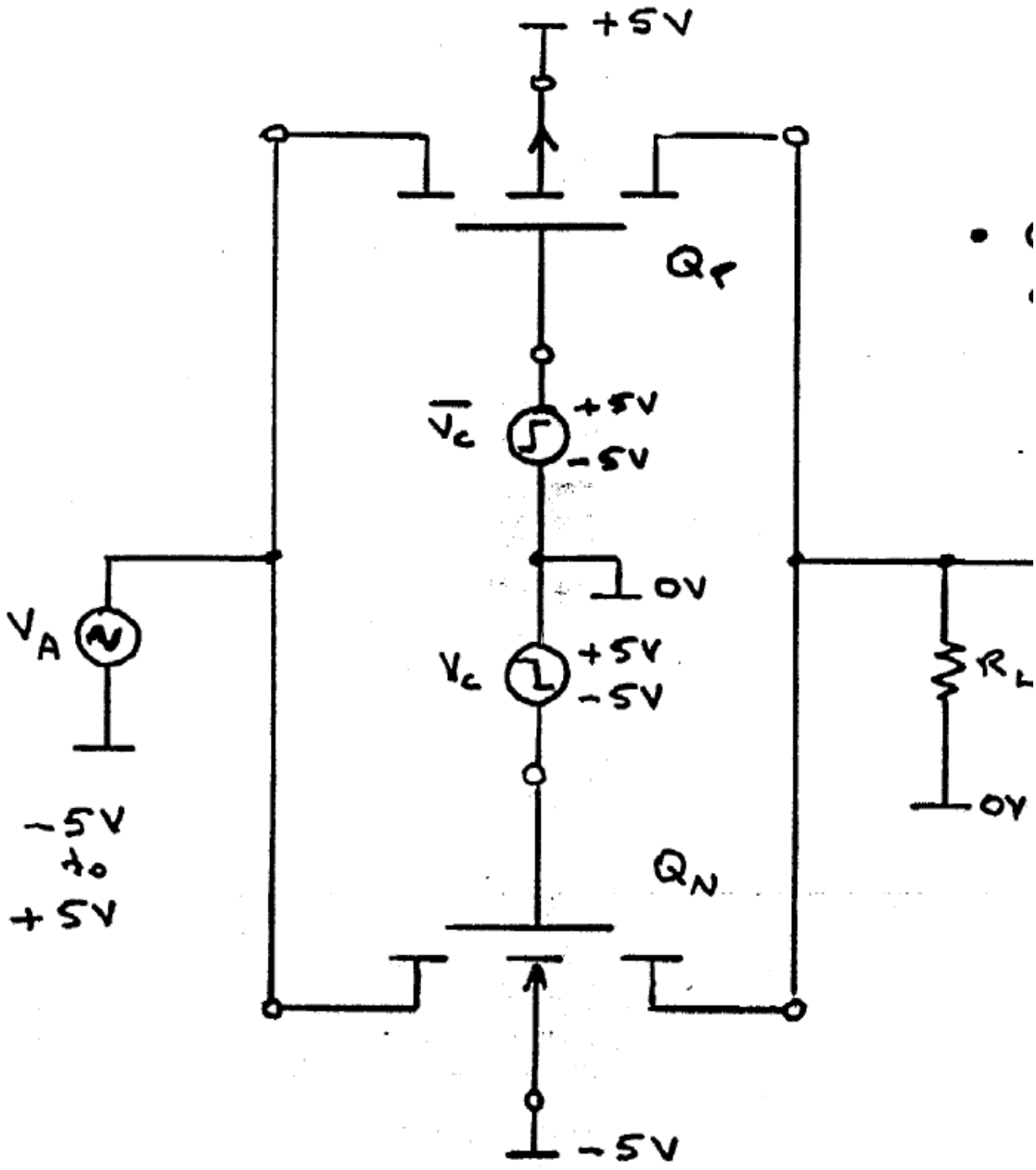

Fig. 6, "CMOS-based Analogue Switch Circuit"

For a CMOS Analogue Switch, let the two MOS devices be matched with $V_{tn} = |V_{tp}| = 2V$ and $k'_n \left(\frac{W}{L}\right)_n = k'_p \left(\frac{W}{L}\right)_p = 100\mu A/V^2$. The load $R_L = 50k\Omega$. Based on this information, calculate the total resistance of the CMOS Analogue Switch in Fig. 6 and the output voltage, V_o, across R_L when the control signal $V_C = +5V$ and $V_A = -5V$. **[4 marks]**

QUESTION 5 (Multistage Amplifiers) [10 marks]

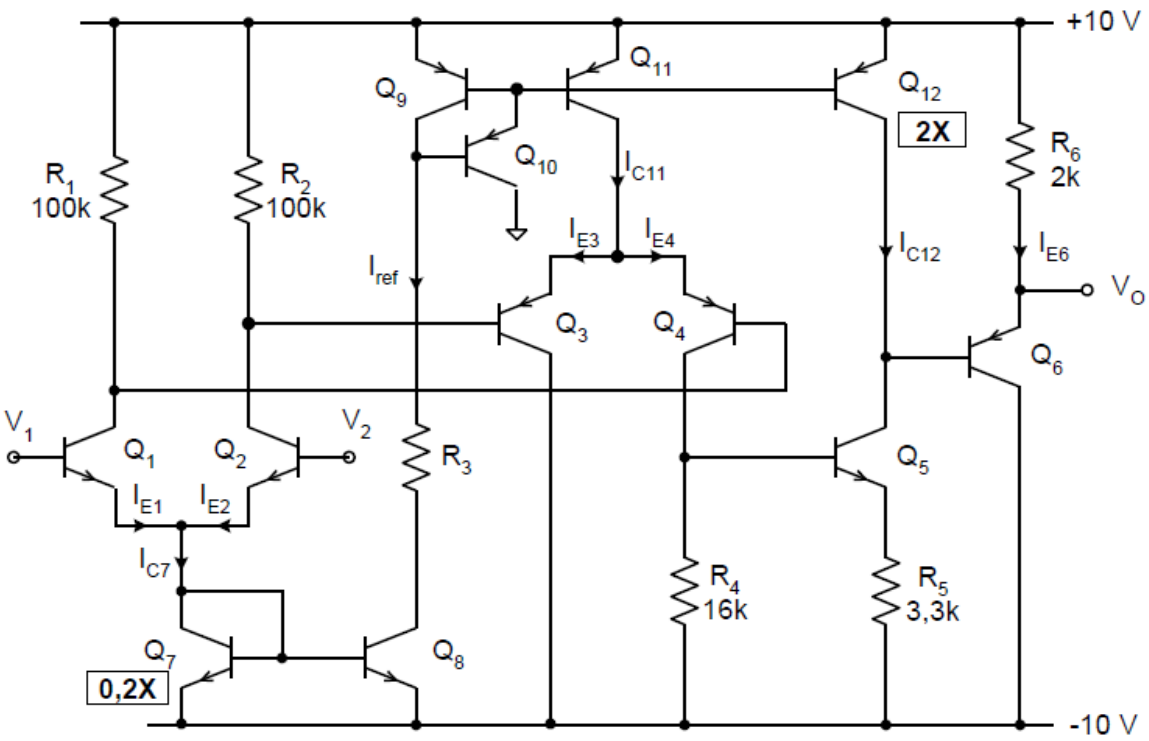

Fig. 7, "Operational Amplifier Circuit"

The circuit diagram of a simple operational amplifier using current mirror biasing is shown in Fig. 7 above. The transistors are all matched except transistors Q_7 and Q_{12} where Q_7 has **one fifth** and Q_{12} **twice** the area of the other transistors. Assume $V_{BE} = V_{EB} = 0.7\ V$ and $V_T = 25\ mV$ for **ALL** NPN and PNP BJTs.

a) Identify and correct the error in the biasing network in Fig. 7. [**2 marks**]

b) Assume external feedback keeps $V_O = 0\,V$ when $V_1 = V_2 = 0V$. Assume that base currents and the Early voltage effect can be neglected for all the transistors, hence, determine the following:

i) Assuming $I_{ref} = 0.5\,mA$, calculate the **total** power dissipated by the passive devices in the **two** differential amplifiers shown in Fig. 7. [**8 marks**]

END OF QUESTIONS

SUPPLIED INFORMATION:

Mirror equations:

Widlar Current Mirror:	$I_o R_E = V_T \ln \frac{I_{ref}}{I_o}$	$R_o = (1 + g_m R'_E) \cdot r_o$	$R'_E = R_E // r_\pi$
Wilson Current Mirror:	$R_o \approx \frac{\beta}{2} \cdot r_o$		

$$r_e = \frac{\alpha}{g_m}, g_m = \frac{I_C}{V_T}$$

MOSFET Equations:

MOSFETS $\quad k' = k'_n = \mu_n C_{ox}$ or $k'_p = \mu_p C_{ox} \qquad \lambda = \frac{1}{V_A} \qquad r_o = \frac{|V_A|}{I_D}$

$$g_m = \sqrt{2k'(W/L)I_D} = k'(W/L)(V_{GS} - V_t) = \frac{2I_D}{V_{GS} - V_t}$$

Triode region $\quad NMOS: V_{DS} < V_{GS} - V_t \qquad i_D = k'\left(\frac{W}{L}\right)\left[(V_{GS} - V_t)V_{DS} - \frac{1}{2}V_{DS}^2\right]$

$\quad PMOS: V_{DS} > V_{GS} - V_t$

Sat. region $\quad NMOS: V_{DS} > V_{GS} - V_t \qquad i_D = \frac{1}{2}k'\left(\frac{W}{L}\right)(V_{GS} - V_t)^2(1 + \lambda V_{DS})$

$\quad PMOS: V_{DS} < V_{GS} - V_t$

Butterworth low-pass equations:

$$\varepsilon = \sqrt{10^{\frac{A_{max}}{10}} - 1} \qquad \omega_o = \omega_P\left(\frac{1}{\varepsilon}\right)^{\frac{1}{N}} \qquad A(\omega) = 10 \cdot \log\left[1 + \varepsilon^2\left(\frac{\omega}{\omega_P}\right)^{2N}\right]$$

$$T(s) = \frac{K \cdot {\omega_o}^N}{(s - p_1)(s - p_2)\cdots(s - p_N)}$$

$$V_{IH} = \frac{1}{8}(5V_{DD} - 2V_t) \qquad V_{IL} = \frac{1}{8}(3V_{DD} + 2V_t) \qquad NM_L = NM_H = \frac{1}{8}(3V_{DD} + 2V_t)$$

$$r_{DS} = \frac{V_{DS}}{I_D} = \frac{1}{k' \cdot \left(\frac{W}{L}\right) \cdot (V_{DD} - |V_t|)}$$

Filter Scaling $\quad R \Rightarrow AR \quad L \Rightarrow \frac{A}{B}L \quad C \Rightarrow \frac{C}{AB} \quad A = \text{impedance factor} \quad B = \text{frequency factor}$

Filter Transformations $\quad LPF(\omega_A) \Rightarrow LPF(\omega_B) \;:\; s \Rightarrow \frac{\omega_A \cdot s}{\omega_B}$

$$LPF(\omega_A) \Rightarrow HPF(\omega_A) \;:\; s \Rightarrow \frac{{\omega_A}^2}{s}$$

2nd order KHN Biquad filter

$$R_F = R_1 \qquad \omega_o = \frac{1}{CR} \qquad Q = \frac{R_2 + R_3}{2R_2} \qquad \frac{V_{BP}}{V_{in}} = \frac{-s \cdot \frac{\omega_o}{Q} \cdot \frac{R_3}{R_2}}{s^2 + s \cdot \frac{\omega_o}{Q} + {\omega_o}^2} \qquad \frac{V_{LP}}{V_{in}} = \frac{\frac{\omega_o^2}{Q} \cdot \frac{R_3}{R_2}}{s^2 + s \cdot \frac{\omega_o}{Q} + {\omega_o}^2}$$

END OF QUESTION PAPER