UNIVERSITY OF KWAZULU-NATAL

School of Engineering: Electrical, Electronic & Computer Engineering

MAIN EXAMINATION: November 2025

Course and Code: **Electrical Principles 2: ENEL2EB-H2**

Duration: THREE hours **Page 1 of 6** **Total marks: 100**

Examiners:	Dr. B Mthethwa	(Analogue Electronics)
	Mr F Mushid	(Digital Electronics)
Independent Moderator:	Prof P Kumar	

General Instructions:

1. This paper contains two sections, **Analogue Electronics** and **Digital Electronics.**
2. Answer each section in a **separate answer book**. Note the name of the section on the front cover of the answer book.
3. Answer **ALL** questions in both sections.
4. You may use any calculator, provided that no text or formulae are present in memory at the start of the examination.
5. **No notes** of any form are allowed in the examination.
6. Show all working in calculations and derivations.
7. Fully label all diagrams and graphs.

Examination Sub-minimum Requirement:

Students must obtain a sub-minimum of 40% in the Analogue section and 40% in the Digital section of the examination.

ANALOGUE ELECTRONICS – answer in a separate book **ANSWER ALL QUESTIONS**

Question A1 [20 marks]

A1.1 **Derive** from first principles an equation for the output voltage V_o in terms of the input voltages V_1 & V_2 for the circuit in Figure A1. Assume the op-amp is ideal. [4]

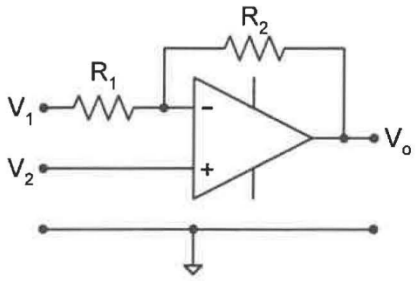


Figure A1

A1.2 The circuit in Figure A1 is then extended as shown in Figure A2 below. Use the result from Q A1.1 to determine an equation for the output voltage V_o in terms of the input voltages V_A & V_B for the circuit in Figure A2. Again assume the op-amps are ideal. Derivations are unnecessary but show all steps. [2]

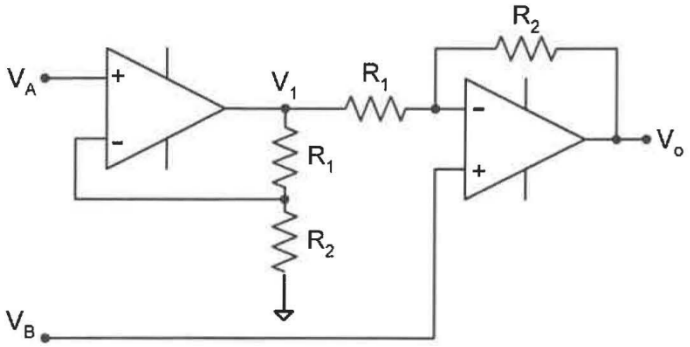


Figure A2

A1.3 The circuits in Figures A1 and A2 both perform a similar function. Identify that function. A popular circuit using three op-amps provides the same common function. Name this circuit and draw a labelled circuit diagram of it. State an equation for the output voltage in terms of the input voltages for this circuit in terms of the labelling you have used. [4]

A1.4 This three op-amp circuit is commonly available as a single IC. The differential voltage gain for such an IC is set via a gain-setting resistor to 40 dB and the CMRR is specified as 100 dB. Determine the output voltage from this circuit if the input voltages V_A and V_B are 4,95 V and 5,05 V respectively. [3]

A1.5.1 An op-amp circuit with two input signals V_1 & V_2 is required to give an output voltage $V_o = -(10 \cdot V_1 + 15 \cdot V_2)$. Design this circuit to use a maximum resistance of 270 kΩ and to include "bias current compensation". Show all relevant calculations and draw the circuit diagram.
The 741 op-amp used has unity gain frequency = 1 MHz, slew-rate limit = 0,5 V/μs, input offset voltage = ±6 mV (max), input bias current = 500 nA (max), and input offset current = 200 nA (max). The dc supply voltages are –9V; 0 V; +9V. [3]

A1.5.2 Determine the transfer function for input signal $V_1 (TF_1 = V_o / V_1)$ as a function of frequency and sketch the Bode magnitude frequency response for this input showing relevant numerical details. [4]

Question A2 [12 marks]

A2.1 A regulated dc power supply consists of a step-down transformer, two silicon rectifier diodes, filter capacitor C, and a simple voltage regulator comprising a series resistor R_S = 25 Ω and a 6 V Zener diode. The transformer primary winding is connected to the 230 Vrms 50 Hz ac mains supply and the centre-tapped secondary winding produces 9 V - 0 V - 9 V rms. Draw the circuit diagram of this supply labelling all relevant voltages and currents. [1]

A2.2 With no external load connected to the power supply, the dc voltage across the capacitor is measured as 11 V using a digital multimeter. Determine the capacitance of the filter capacitor and the maximum power dissipated in R_S. The Zener diode current is to be limited by series resistor R_S to 80% of the maximum rated Zener current (I_{Zmax}). Determine the power rating required for the Zener diode. [4]

A2.3 Determine the diode conduction angle in degrees, the peak diode currents and the PIV rating required for the rectifier diodes. Hence simply sketch the capacitor voltage and diode current waveforms expected showing relevant numerical values. [5]

A2.4 If the Zener diode current is not to fall below 20% of I_{Zmax}, determine the minimum load resistance R_L that may be connected to the output of the regulator. Briefly explain what will happen if the load resistance is reduced below this minimum value. [2]

Question A3 [18 marks]

A3.1 The two-stage BJT amplifier circuit in Figure A3 uses the same dc bias circuit for each stage. For this bias circuit, assuming for the silicon BJTs V_{BE} = 0,7 V in active mode and β = 250, determine the BJT currents I_E and I_C and voltage V_{CE}. [4]

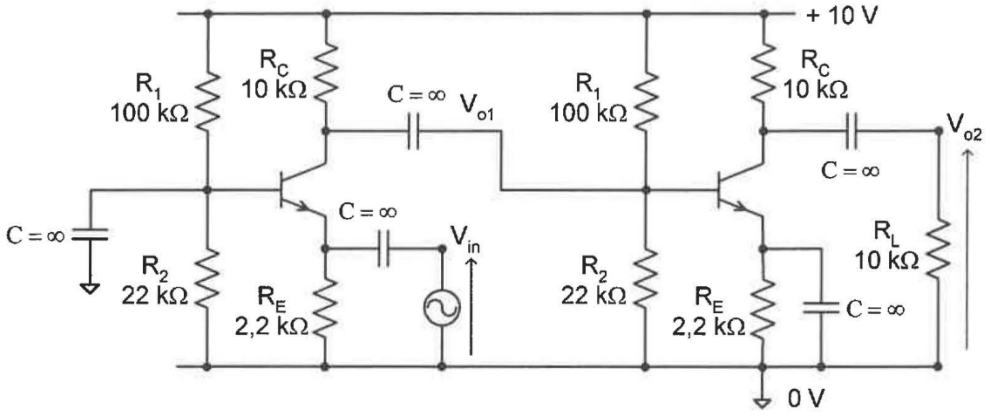


Figure A3

A3.2 Identify the BJT configuration for each stage and draw an ac small-signal equivalent circuit for this amplifier using suitable BJT models assuming V_T = 25 mV and $V_A = \infty$. The capacitor reactances may all be taken as negligible at signal frequencies. Hence determine the overall voltage gain V_o/V_{in}. [9]

A3.3 Redesign the dc bias circuit used in Figure A3 to give a dc collector current of approximately 3 mA assuming the same BJT properties and application. Show all design calculations and select nearest E12 standard resistor values. [5]

E12 series:	10	12	15	18	22	27	33	39	47	56	68	82

End of Analogue Electronics Section

DIGITAL ELECTRONICS – answer in a separate book **ANSWER ALL QUESTIONS**

Question D1 [25 marks]

D1.1 Perform the following operations:

a) Convert $B9FD_{16}$ to decimal.

b) Convert 101011101.01001_2 to hexadecimal.

c) Convert 122.45_{10} to octal.

d) Subtract 101001_2 from 10011_2 using 2's complement.

[5]

D1.2 Using the K-map procedure, implement the optimum solution of the following Boolean function:

$$F(A, B, C, D) = \sum(1,2,3,5,6,8,9,10,13)$$

[8]

D1.3 The table TD1 below shows a truth table for a system with three inputs and two outputs, F1 and F2. Design a simple PLD to implement the system.

Table TD1

x	y	z	F1	F2
0	0	0	0	1
0	0	1	1	1
0	1	0	1	1
0	1	1	0	0
1	0	0	0	1
1	0	1	1	0
1	1	0	0	1
1	1	1	1	0

[6]

D1.4 Write down the truth table for the circuit in figure D1 below. Hence, minimize the circuit using the K-map method.

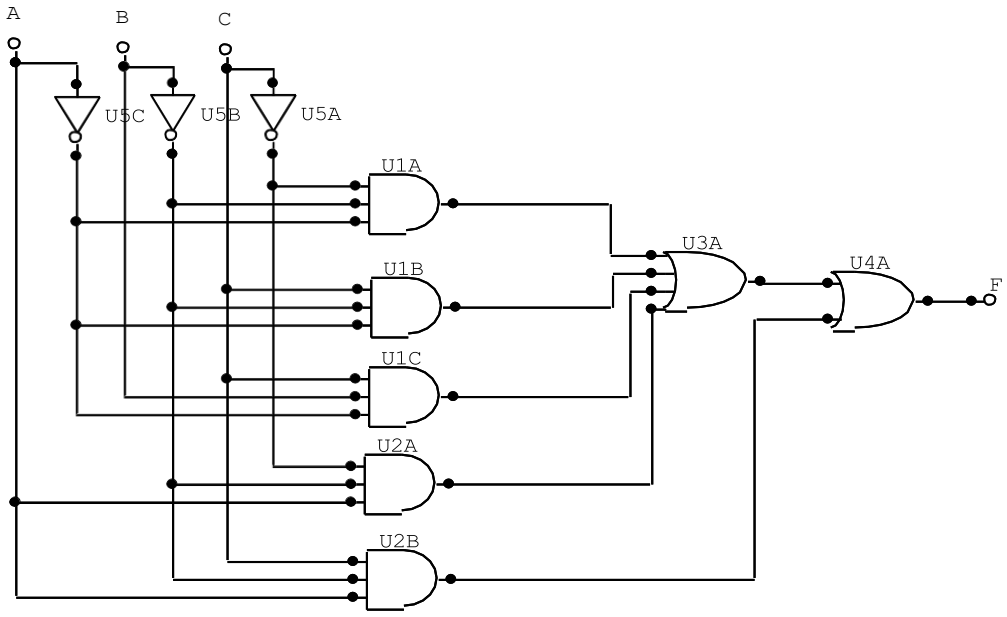


Figure D1

[6]

Question D2 [25 marks]

D2.1 Implement the following Boolean function with a Multiplexer.

$F(A,B,C,D) = \sum(1,2,3,5,6,8,9,10,13)$.

[5]

D2.2.

a) What is the difference between an encoder and a decoder? Design a 5 X 32 decoder with 3 X 8 decoders (e.g., the 74138 decoder) and a 2 X 4 decoder. You can use block diagrams in your design. State clearly any assumptions made. [4]

b) The figure D2 below shows a basic J-K flip-flop. Write down its characteristic table and describe how the circuit works. Why is this circuit considered to be an improvement to R-S flip-flop? [4]

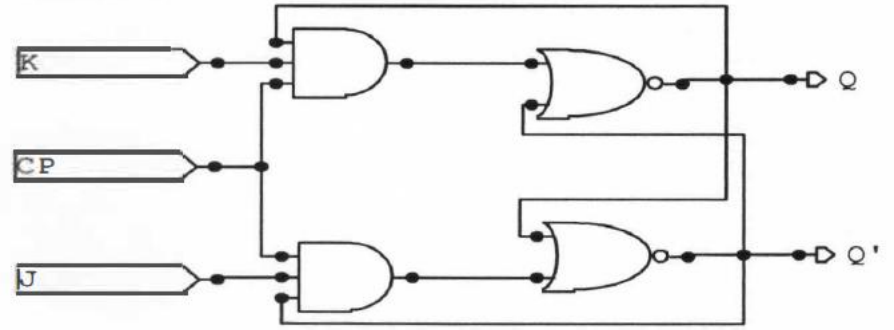


Figure D2

D2.3

The incomplete table 1 below is an attempt to design a J-K flip-flop based up counter, which counts in the order, 1, 3, 5, 7, 9 and then 11. Complete this design by first completing the respective values of J_3K_3, J_1K_1 and J_0K_0 for all the above counts. Simplify for J_3K_3, J_1K_1 and J_0K_0 and then draw the circuit diagram. (Note that all counts higher than 11 represent don't care conditions).

Table 1

Decimal Count	Present Sate	Next Sate	Flip-Flop Input			
	$Q_3Q_2Q_1Q_0$	$Q_3Q_2Q_1Q_0$	J_3K_3	J_2K_2	J_1K_1	J_0K_0
1	0001	0011				
3	0011	0101				
5	0101	0111				
7	0111	1001				
9	1001	1011				
11	1011	0001				

[12]

End of Question paper